Supertex inc.

P-Channel Enhancement-Mode Lateral MOSFET

Ordering Information

BV$_{DSS}$ / BV$_{DGS}$	R$_{DS(ON)}$ (max)	I$_{D(ON)}$ (min)	V$_{GS(th)}$ (max)	Order Number / Package		
				TO-92	SO-8	Die
-16.5V	1.5Ω	-1.25A	-1.0V	LP0701N3	LP0701LG	LP0701ND

Features

❏ Ultra low threshold
❏ High input impedance
❏ Low input capacitance
❏ Fast switching speeds
❏ Low on resistance
❏ Freedom from secondary breakdown
❏ Low input and output leakage
❏ Complementary N- and P-channel devices

Applications

❏ Logic level interfaces
❏ Solid state relays
❏ Battery operated systems
❏ Photo voltaic drives
❏ Analog switches
❏ General purpose line drivers

Absolute Maximum Ratings

Drain-to-Source Voltage	BV$_{DSS}$
Drain-to-Gate Voltage	BV$_{DGS}$
Gate-to-Source Voltage	± 10V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Advanced MOS Technology

These enhancement-mode (normally-off) transistors utilize a lateral MOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown. The low threshold voltage and low on-resistance characteristics are ideally suited for hand held battery operated applications.
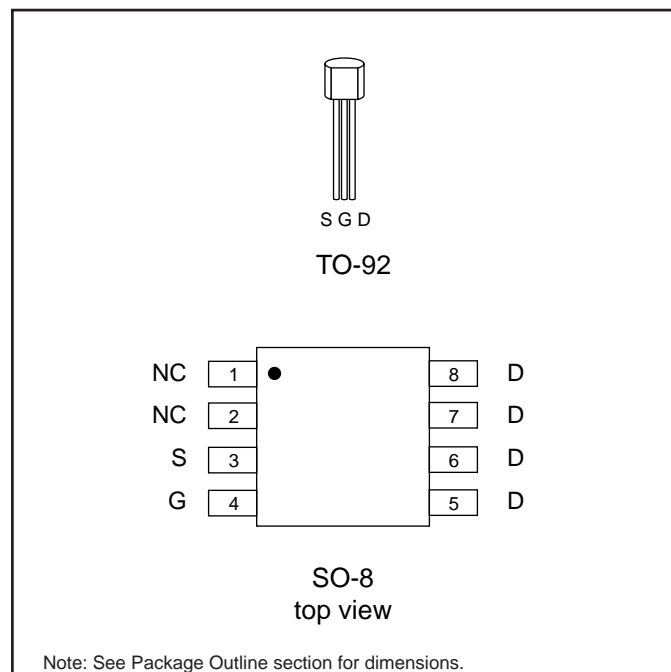
Package Options

S G D

TO-92

NC	1	●	8	D
NC	2		7	D
S	3		6	D
G	4		5	D

SO-8
top view

Note: See Package Outline section for dimensions.

Thermal Characteristics

Package	I$_D$ (continuous)*	I$_D$ (pulsed)*	Power Dissipation @ T$_C$ = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I$_{DR}$	I$_{DRM}$*
TO-92	-0.5A	-1.25A	1W	125	170	-0.5A	-1.25A
SO-8	-0.7A	-1.25A	1.5W†	83	104†	-0.7A	-1.25A

* I$_D$ (continuous) is limited by max rated T$_j$.
† Mounted on FR4 board, 25mm x 25mm x 1.57mm.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV$_{DSS}$	Drain-to-Source Breakdown Voltage	-16.5			V	V$_{GS}$ = 0V, I$_D$ = -1mA
V$_{GS(th)}$	Gate Threshold Voltage	-0.5	-0.7	-1.0	V	V$_{GS}$ = V$_{DS}$, I$_D$ = -1mA
ΔV$_{GS(th)}$	Change in V$_{GS(th)}$ with Temperature			-4.0	mV/°C	V$_{GS}$ = V$_{DS}$, I$_D$ = -1mA
I$_{GSS}$	Gate Body Leakage			-100	nA	V$_{GS}$ = ±10V, V$_{DS}$ = 0V
I$_{DSS}$	Zero Gate Voltage Drain Current			-100	nA	V$_{DS}$ = -15V, V$_{GS}$ = 0V
				-1.0	mA	V$_{DS}$ = 0.8 Max Rating, V$_{GS}$ = 0V, TA = 125°C
I$_{D(ON)}$	ON-State Drain Current		-0.4		A	V$_{GS}$ = V$_{DS}$ = -2V
		-0.6	-1.0			V$_{GS}$ = V$_{DS}$ = -3V
		-1.25	-2.3		A	V$_{GS}$ = V$_{DS}$ = -5V
R$_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		2.0	4.0	Ω	V$_{GS}$ = -2V, I$_D$ = -50mA
			1.7	2.0		V$_{GS}$ = -3V, I$_D$ = -150mA
			1.3	1.5		V$_{GS}$ = -5V, I$_D$ = -300mA
ΔR$_{DS(ON)}$	Change in R$_{DS(ON)}$ with temperature			0.75	%/°C	V$_{GS}$ = -5V, I$_D$ = -300mA
G$_{FS}$	Forward Transconductance	500	700		m℧	V$_{DS}$ = -15V, I$_D$ = -1A
C$_{ISS}$	Input Capacitance		120	250		
C$_{OSS}$	Common Source Output Capacitance		100	125	pF	V$_{GS}$ = 0V, V$_{DS}$ = -15V, f = 1MHz
C$_{RSS}$	Reverse Transfer Capacitance		40	60		
t$_{d(ON)}$	Turn-ON Delay Time			20	ns	
t$_r$	Rise Time			20		V$_{DD}$ =-15V, I$_D$ = -1.25A, R$_{GEN}$ = 25Ω
t$_{d(OFF)}$	Turn-OFF Delay Time			30		
t$_f$	Fall Time			30		
V$_{SD}$	Diode Forward Voltage Drop		-1.2	-1.5	V	V$_{GS}$ = 0V, I$_{SD}$ = -500mA

Note 1:   All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
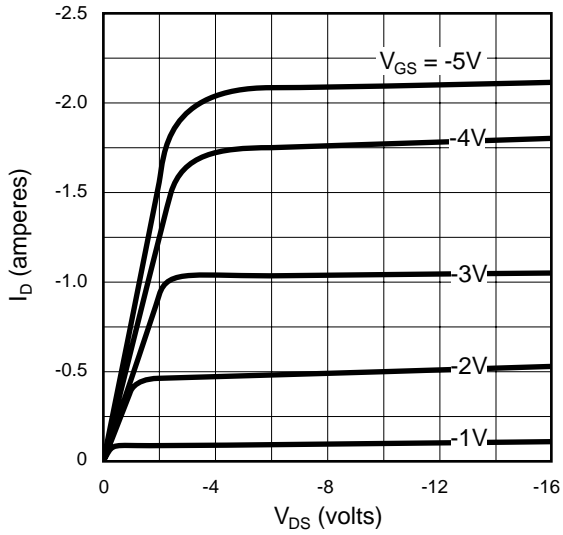Note 2:   All A.C. parameters sample tested.
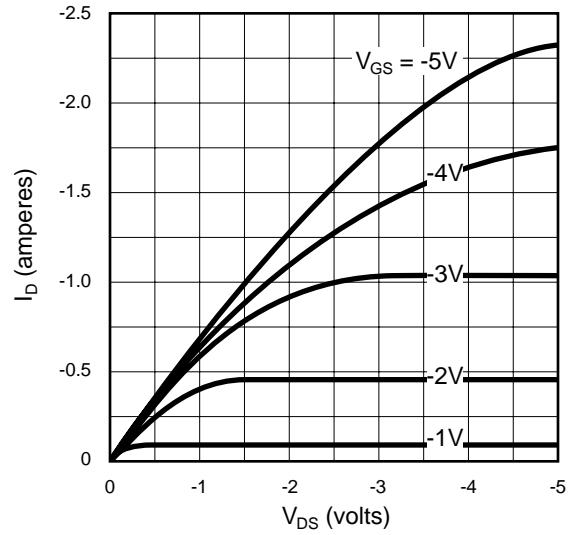
Switching Waveforms and Test Circuit
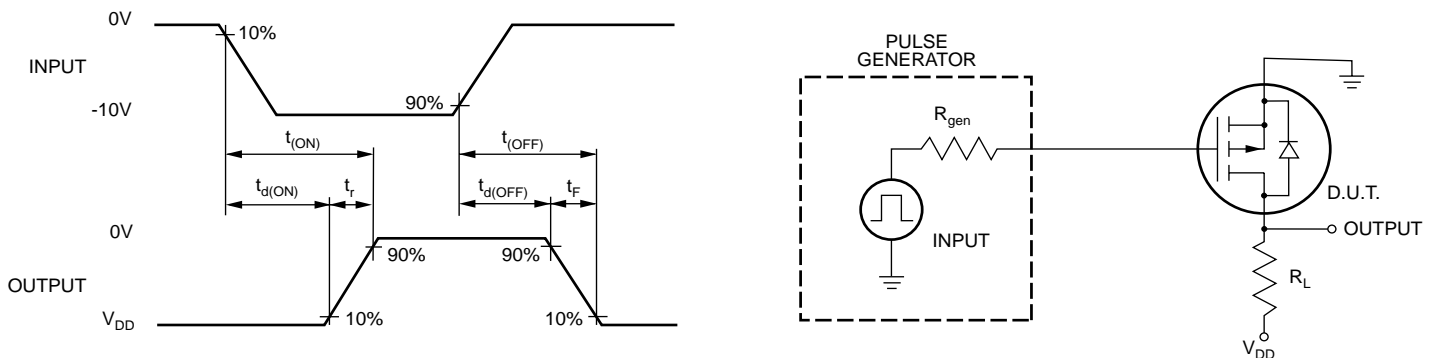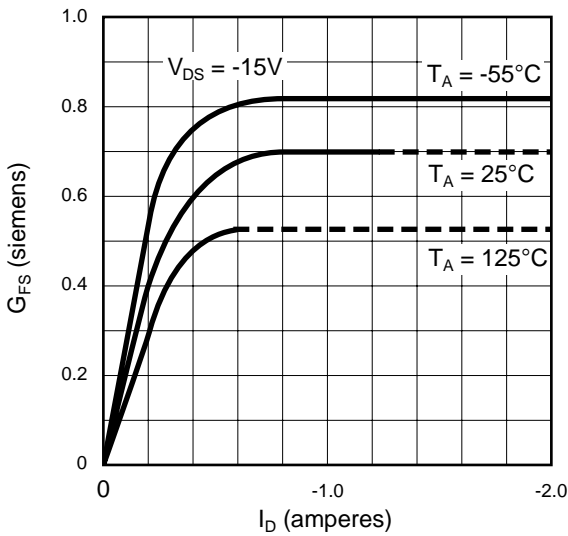
Typical Performance Curves

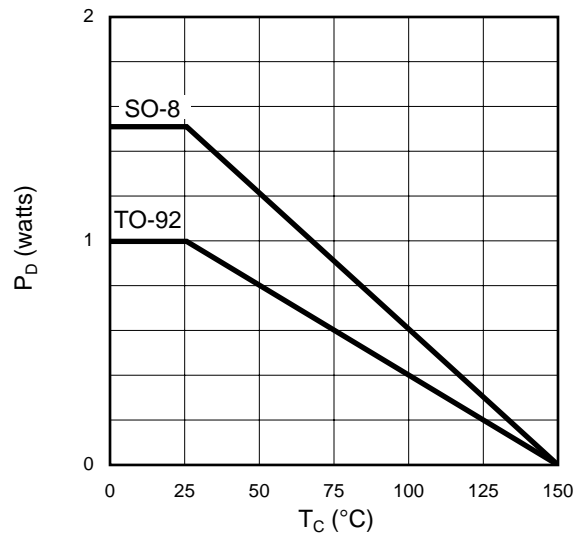### Output Characteristics

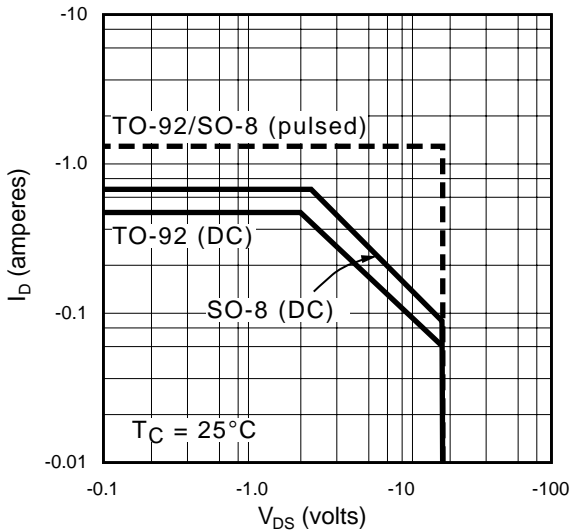### Saturation Characteristics

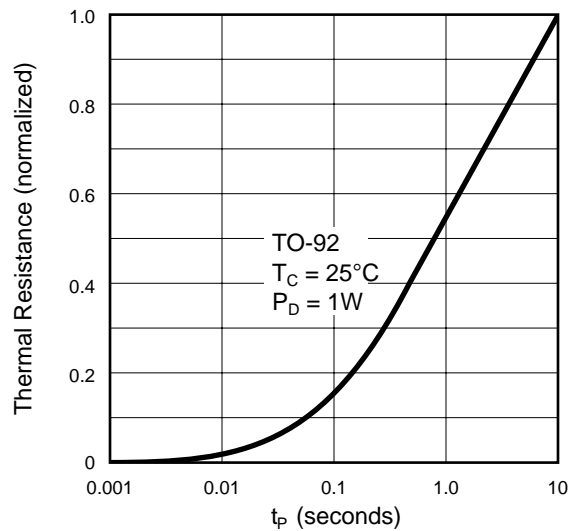### Transconductance vs. Drain Current

Power Dissipation vs. Case Temperature

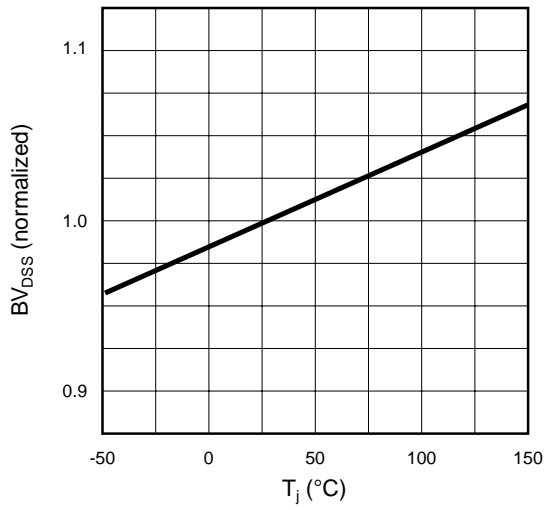### Maximum Rated Safe Operating Area
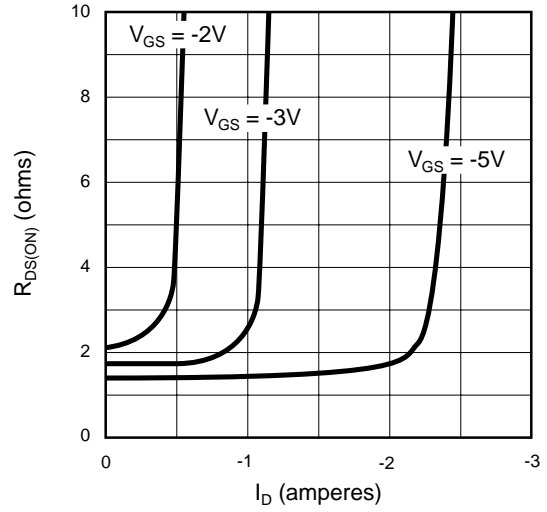

Thermal Response Characteristics
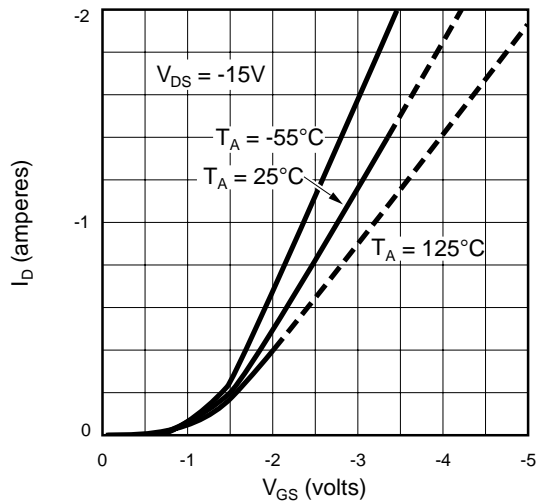
Typical Performance Curves

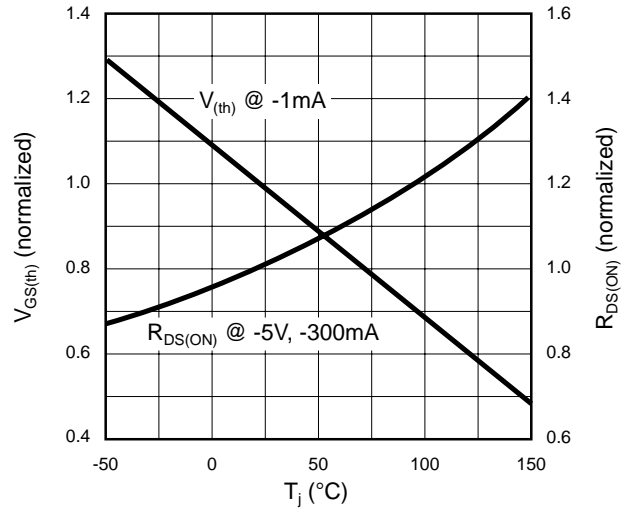BV$_{DSS}$ Variation with Temperature
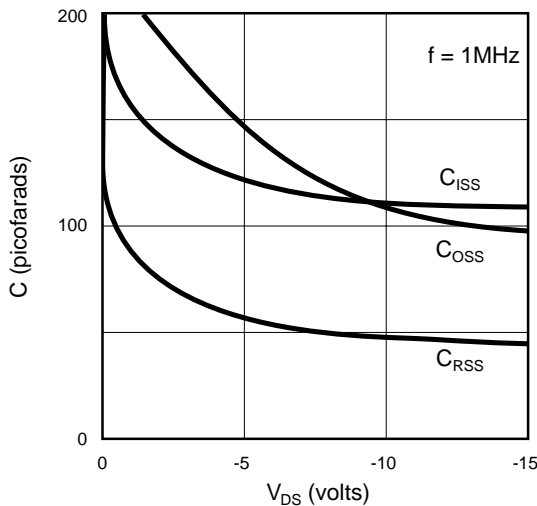
On-Resistance vs. Drain Current

Transfer Characteristics

V$_{(th)}$ and R$_{DS}$ Variation with Temperature

Capacitance vs. Drain-to-Source Voltage

Gate Drive Dynamic Characteristics

01/06/03

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